Intel® 82801DB I/O Controller Hub 4 (ICH4)

Whitepaper

May 2002

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Revision History

Rev. No.	Description	Rev. Date
-001	Initial Release.	May 2002

Overview Product Features

- **PCI Bus I/F**
  - Supports PCI Rev 2.2 Specification at 33 MHz
  - 133 Mbytes/sec maximum throughput
  - Supports up to 6 master devices on PCI
  - One PCI REQ/GNT pair can be given higher arbitration priority (intended for external 1394 host controller)
  - Support for 44-bit addressing on PCI using DAC protocol
- **Integrated LAN Controller**
  - WfM 2.0 and IEEE 802.3 Compliant
  - LAN Connect Interface (LCI)
  - 10/100 Mbit/sec Ethernet Support
- **Integrated IDE Controller**
  - Supports "Native Mode" Register and Interrupts
  - Independent timing of up to 4 drives, with separate Primary and Secondary IDE cable connections
  - Ultra ATA/100/66/33, BMIDE and PIO modes
  - Tri-state modes to enable swap bay
- **USB**
  - Includes 3 UHCI Host Controllers, increasing the number of external ports to six
  - New: Includes 1 EHCI High-speed USB 2.0 Host Controller that supports all six ports
  - New: Supports a USB 2.0 High-speed Debug Port
  - Supports wake-up from sleeping states S1-S5
  - Supports legacy Keyboard/Mouse software
- **AC'97 for Audio**
  - New: Supports AC '97 Spec. Rev. 2.3
  - New: Third AC_SDATA_IN Line for three codec support
  - New: Independent bus master logic for 7 channels (PCM In/Out, Mic 1 Input, Mic 2 Input, Modem In/Out, S/PDIF Out)
  - Separate independent PCI functions for Audio and Modem
  - Support for up to six channels of PCM audio output (full AC3 decode)
  - Supports wake-up events
- **Interrupt Controller**
  - Support up to 8 PCI interrupt pins
  - Supports PCI 2.2 Message Signaled Interrupts
  - Two cascaded 82C59 with 15 interrupts
  - Integrated I/O APIC capability with 24 interrupts
  - Supports Serial Interrupt Protocol
  - Supports Processor System Bus interrupt delivery
- **New: 1.5 V operation with 3.3 V I/O**
  - 5V tolerant buffers on IDE, PCI, USB Over-current and Legacy signals
- **Timers Based on 82C54**
  - System timer, Refresh request, Speaker tone output
- **Power Management Logic**
  - ACPI 2.0 compliant
  - ACPI-defined power states (C1-C2, S3-S5)
  - ACPI Power Management Timer
  - PCI CLKRUN# and PME# support
  - SMI# generation
  - All registers readable/restorable for proper resume from 0V suspend states
- **External Glue Integration**
  - Integrated Pull-up, Pull-down and Series Termination resistors on IDE, CPU I/F
  - Integrated Pull-down and Series resistors on USB
- **Enhanced Hub I/F buffers improve routing flexibility** (Not available with all Memory Controller Hubs)
- **Firmware Hub (FWH) I/F supports BIOS Memory size up to 8 Mbytes**
- **Low Pin Count (LPC) I/F**
  - New: No ISA/X-Bus support
  - Supports two Master/DMA devices.
- **Enhanced DMA Controller**
  - Two cascaded 8237 DMA controllers
  - PCI DMA: Supports PC/PCI — Includes two
  - PC/PCI REQ#/GNT# pairs
  - Supports LPC DMA
  - Supports DMA Collection Buffer to provide Type-F DMA performance for all DMA channels
- **Real-Time Clock**
  - 256-byte battery-backed CMOS RAM
- **System TCO Reduction Circuits**
  - Timers to generate SMI# and Reset upon detection of system hang
  - Timers to detect improper CPU reset
  - Integrated CPU frequency strap logic
  - Supports ability to disable external devices
- **SMBus***
  - New: Hardware Packet Error Checking
  - New: Supports SMBus 2.0 Specification
  - Host interface allows CPU to communicate via SMBus
  - Slave interface allows an external Microcontroller to access system resources
  - Compatible with most 2-Wire components that are also I2C* compatible
- **GPIO**
  - TTL, Open-Drain, Inversion
- **Package 31x31 mm 421 BGA**

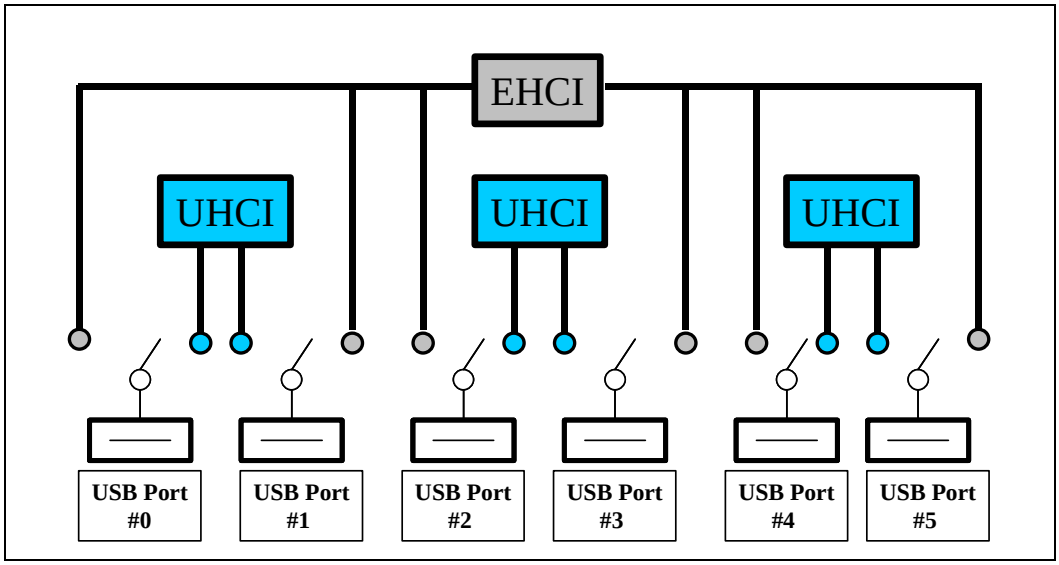
1 New Product Features

1.1 Hi-Speed USB 2.0

The Intel® 82801DB I/O Controller Hub 4 (ICH4), hereafter referred to ICH4, contains an Enhanced Host Controller Interface (EHCI) compliant host controller which supports USB high-speed signaling. Hi-speed USB 2.0 allows data transfers up to 480 Mb/s- 40 times faster than full-speed USB. The ICH4 also contains three Universal Host Controller Interface (UHCI) controllers that support USB full-speed and low-speed signaling.

The ICH4 supports 6 USB 2.0 ports. All six ports are high-speed, full-speed, and low-speed capable. ICH4s port-routing logic determines whether a USB port is controlled by one of the UHCI controllers or by the EHCI controller.

Figure 1: ICH4 USB 2.0 Port Routing



The advantages of the ICH4's integrated USB implementation can be grouped into three general categories; Performance, Platform Capabilities, and Compatibility.

1.2 Performance

Intel's Enhanced Host Controller has been designed for optimal performance to meet the demands of not only today's devices but also the increased demands expected from hi-speed USB2.0 devices for years to come. With integration into the chipset, the special needs of the host controller's memory access patterns can be optimized through internal protocols, data paths, and arbiters that are not possible or cost-effective for non-integrated implementations.

1.2.1 Concurrent Pipelined Operation

The USB Host Controller Specifications are defined such that control structures (Frame Lists, Queue Heads, and Transfer Descriptors) and data buffers are maintained in system memory. Software communicates with the host controller through these memory structures, thereby minimizing system processor delays for directly accessing the host controller (and USB device) registers. In this environment, the key to USB performance is the ability of the host controller to access memory effectively.

Intel's integrated USB Host Controllers operate concurrently in a pipelined manner to maximize memory accessibility and the corresponding data rates on the USB wires. All three classic USB controllers can independently read and write memory concurrently for low-speed and full-speed devices. Additionally, the EHCI (High-Speed) USB host controller implements two independent Memory Access engines for the Asynchronous and Periodic schedules, respectively. These two independent EHCI engines can further pipeline memory reads to get a jump-start on transactions following the current one. Therefore, the USB host controllers can simultaneously have seven reads in progress for 7 different transactions (see table below). The number of ongoing USB writes that may be pending at any given instant is much larger than reads due to the numerous buffers between the USB interface and the memory interface.

Table 1: Concurrent USB Host Controller Reads

Initiator	Number of Concurrent Reads	Comments
Universal Host Controllers	3	Three independent UHCI Controllers for low- and full-speed (12Mb/s) transactions
Enhanced Host Controller	4	Two pipelining engines for high-speed (480Mb/s) transactions
Total:	7	

In order to efficiently process the high number of concurrent read requests from USB (and other agents in the platform) the chipset uses queuing and split-transaction protocols on its interfaces. Split-transaction operation was not inherent in the original PCI specification. As a result, the burden to support a high number of concurrent read requests is large in the 32-bit, 33 MHz PCI protocol. PCI-based USB host controllers typically do not achieve the same degree of concurrent pipelined operation as the ICH4.

1.2.2 High Bandwidth Interface to System Memory

The ICH4 integrates the USB host controller agents on the 266MB/s hub interface that connects to the memory controller. With twice the available bandwidth of 32-bit, 33 MHz PCI devices, the hub interface can easily handle the traffic associated with the 6 USB Ports (and the control structure overhead) concurrently with a fully utilized PCI bus. External PCI-based host controllers can become impacted by other high-bandwidth PCI agents due to the limited bandwidth that must be shared on PCI.

1.3 Quality of Service

The USB specification includes support for isochronous data types (a stream of data with packets scheduled at regular, periodic intervals). The ICH4 provides information with the isochronous USB memory requests to avoid isochronous failures under common system-stalled conditions. The isochronous information is used to optimize arbiters and to allow progress through dedicated command and data paths while the normal paths may be stalled. With today's PC designs, this can only be achieved when the requesting agent (USB) is tightly integrated with the system logic.

Additionally, the integrated High-Speed EHCI Host Controller provides enough buffering to fully consume up to four maximum-size packets. This ensures that packet overruns and underruns do not occur, while at the same time allowing for pipelining of both transmit and receive packets for both asynchronous and periodic schedules.

One example in which the integrated Host Controller continues to provide isochronous service when PCI-based devices are stalled is when an older PCI card is operating in the system. Prior to the 2.1 revision of the PCI specification, initiators were permitted to not re-attempt a delayed transaction on PCI. If such a device is placed in the platform, large delays can be created on the PCI bus for other initiators while the host controller waits for a discard timer to clear out the delayed transaction. Additionally, cards that are not compliant to the 2.2 revision of the PCI specification may insert large numbers of target wait states on data that is directed to them. Revision 2.2 of the PCI spec added text to help limit the delays on a long sequence of posted writes, for example. However, even with the spec change, cards can be compliant and still cause long delays to other devices on the PCI bus because of its shared nature. The integrated Host Controllers in the ICH4 can continue to receive and transmit normally when these delays are occurring.

1.4 Platform Capabilities

The second major advantage of the integrated USB host controller in the ICH4 is the various platform capabilities that are provided. Many of the optional EHCI specification features are included in the Intel implementation to enhance the value of USB in the platform.

1.4.1 Integrated Debug Port

The ICH4 includes a USB 2.0-based Debug Port specified as an option in the EHCI specification's appendix. This port is a generic, discoverable function that allows host-based software to interleave small transfers on one of the USB ports. The implementation allows the transfers to occur with or without a USB 2.0 host software driver on the system and is intended to help speed up the development and debug of any software running on the system. It can replace the debug

capabilities that have been provided previously on older legacy interfaces, thereby helping to eliminate big, high-voltage, low-bandwidth connectors.

The USB 2.0-based debug port is operated by reading and writing four memory-mapped registers in the host controller that are addressed above the rest of the registers in the EHCI memory range. The software reads and writes the debugger device connected to the USB port with up to 64 bits of data at a time.

1.4.2 BIOS and Boot Support

The ICH4 fully implements the optional USB Legacy Support registers as defined in the EHCI specification. These registers allow the BIOS to temporarily control the host controller using System Management Interrupts (SMI's), as opposed to standard interrupts, before the OS-based EHCI driver has loaded. The mechanism also provides semaphore bits to achieve a graceful hand-off from the BIOS to OS driver and vice versa.

1.4.3 Full Support for Platform Power Management

In addition to the USB host controllers, the ICH4 contains much of the logic that controls platform power management states. As a result, the USB controllers benefit from the multiple power wells already available on chip, allowing full support for waking from device-suspend and system-sleep states. Most of the controllers' logic is powered off (except for resume-detection logic) in system sleep states, thereby helping to save power.

The optional Port Wake Capability Register in the EHCI specification is also implemented in the ICH4. This register can be used by the BIOS to communicate to the OS which ports are not wake-capable if the platform does not support waking from all 6 ports. This may be the case if power is not provided to the ports in a low-power system state, for example. The EHCI specification and ICH4 also allow the platform to customize the type of events that can wake the system.

Additionally, the EHCI Host Controller implements PCI Power Management, with support for the D0, D3hot, and D3cold device states.

1.5 Compatibility

The ICH4 provides USB configuration options to provide compatibility in various platform environments. The integrated USB 2.0 implementation utilizes the stable UHCI host controllers, has been rigorously validated, and is supported by various documents. And because it is integrated into the chipset, its operation is tested extensively with all of the other platform functionality contained in the PC core-logic. Intel's integrated USB 2.0 implementation emphasizes compatibility with USB devices, software, and the PC platform.

1.5.1 Configurable Architecture

The ICH4 can be configured through BIOS to support fewer than 6 USB Ports and report this correctly to the operating system. This may be useful in the event that a platform does not have room to route or to provide connectors for all of the ports. It could also be used for offering a value product with fewer connectors while using the same board layout as the full-featured platform. Reducing the number of reported ports is achieved by writing to an access bit, which

then allows the EHCI Host Controller Structural Parameters register to be over-written. This Structural Parameters register reports the total number of ports supported and the number of companion classic host controllers to the driver software. The companion classic host controllers can also be hidden from plug-and-play software through BIOS for situations in which its ports are not available in the system.

1.5.2 Integrated UHCI Controllers

Retaining the Intel UHCI host controllers that have been validated and tested on high volume platforms minimizes incompatibility risks with older full-speed and low-speed USB1.1 devices. This implementation option within the EHCI specification allows the newer high-speed host controller design to have minimum impact on the existing host controllers. Backwards compatibility with full-speed and low-speed USB1.1 devices was a primary requirement of the USB 2.0 initiative.

1.5.3 Extensive Validation and Support

Intel is a key developer and enabler of the USB 2.0 and EHCI specification. As a result, the development teams within the company have worked closely with software developers, device vendors, and compliance work groups to help ensure compatibility. Additionally, Intel has extensively validated the USB 2.0 Host Controller. Special test fixtures and validation environments have been developed and used to stress the design in both pre-silicon and post-silicon phases of the design. This has allowed for thorough testing to compliance of the specifications, not just interoperability with the limited behavior of currently available devices.

The Analog portion of the high-speed USB interface has been carefully characterized and improved through test chips and in real motherboard environments. This circuitry integrates components that had previously been required on the PC board and provides advanced features such as configuration registers to tune electrical characteristics and self-compensating circuits; all of which help provide compatibility within the particular operating environment.

Intel provides technical support and documents with all of its chipset products. The USB 2.0 functionality is no exception; white papers, BIOS specifications, and External Design Specifications are available to help with using the integrated USB 2.0 functionality in the ICH4.

1.6 AC ‘97

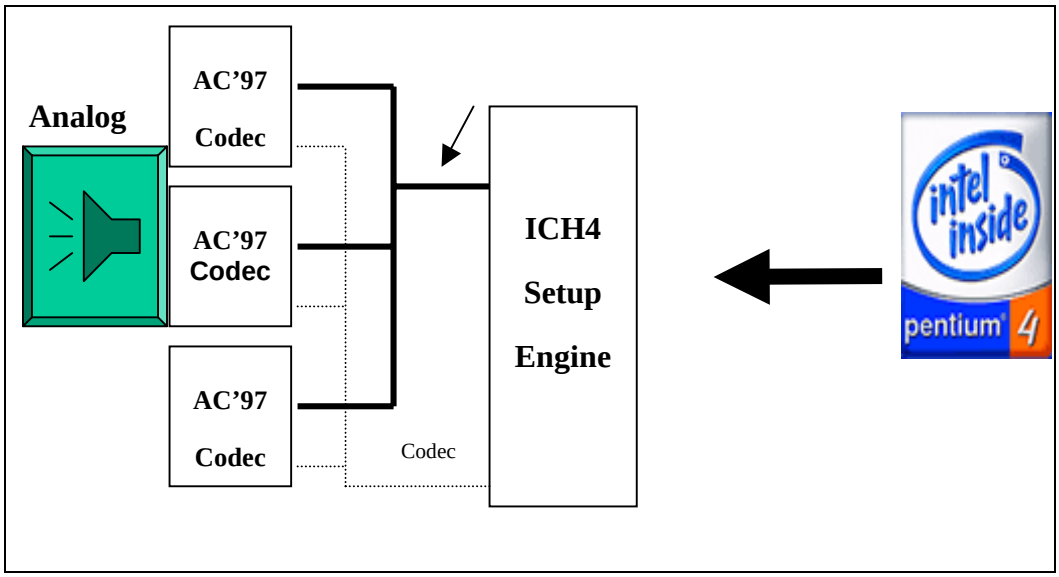
Several enhancements have been made to the ICH4 AC’97 audio controller to raise the performance baseline of integrated audio. These enhancements are:

- Support for 20-bit PCM audio output
- Hardware acceleration of S/PDIF digital output
- Support for separate and uniquely identifiable audio input
- Use of memory mapped space for programming
- Support for PCI Power Management

Independent Simultaneous SPDIF and PCM output

Figure 2: Independent Simultaneous SPDIF and PCM output

Digital Audio



1.6.1 Support for 20-bit Analog Audio Output

The ICH4 allows for 20-bit audio output when in 2 channel, 4 channel, or 6 channel modes. Supporting 20-bit audio allows for higher end audio to be played in the basic platform with a supporting codec, thus improving sound quality and dynamic range to end-users. This increases the capability of the platform to over 98dB from 92dB on previous platforms, depending on the codec solution. In addition, the ICH4 supports up to 96KHz sampling (a consumer electronics CD player is typically 16 bit and 48KHz sampling).

1.6.2 Hardware Acceleration of S/PDIF Digital Output

Previous incarnations of the AC'97 controller in ICH did not have any dedicated hardware for S/PDIF output. Analog streams (PCM) and digital streams (S/PDIF) are separate and independent in the audio subsystem of the PC.

To support digital audio in older ICH's, driver software had to merge these two streams into one by performing buffer copies, before presenting them to the ICH. As an example, 2-channel stereo PCM playing concurrently with S/PDIF meant that software had to configure the ICH as 4-channel audio and perform a buffer copy to place the PCM and S/PDIF digital data into one memory location for the ICH to fetch. Driver software then would also have to configure the AC'97 codec to extract this information into its analog and digital components.

The ICH4 has been enhanced by creating an independent DMA engine solely for S/PDIF digital data. Driver software no longer has to perform buffer copies, and the S/PDIF digital data can be placed on any available AC'97 interface slot. By removing the buffer copies, the CPU is available for other processing tasks, and by having an independent slot for S/PDIF digital data, the digital data is not affected if the PCM data changes. The end user benefits from the additional independent DMA engine by allowing two simultaneous different audio streams to be played at the same time.

1.6.3 Support for Separate and Uniquely Identifiable Audio Input

The ICH4 has added 2 additional DMA engines for a separate audio input. These engines are for microphone and stereo in. With these additional engines, the AC'97 host controller in ICH4 can uniquely identify an audio input source. The dual DMA engines enable more complex usage enhancements. Additional inputs enable stereo microphone arrays for enhanced speech applications through additional echo cancellation and noise reduction.

1.6.4 Use of Memory Mapped Space for Programming

Previous generations of the AC'97 controller in ICH used I/O space for programming of both the host and codec. The ICH4 AC'97 controller maintains the I/O space for backwards compatibility with older drivers, and also adds a memory space to access the same registers. Use of memory space will greatly increase the performance of many programming operations, leaving the CPU available for other tasks.

1.6.5 PCI Power Management

Previous generations of the AC'97 audio controller in the ICH required the use of ACPI power management. This required a larger BIOS burden to develop code for each individual platform. In the ICH4, this power management has been replaced with PCI power management, both for the audio and modem functions. By using PCI power management, the BIOS burden is greatly reduced and existing operating system routines can perform the power management tasks.

In addition, wake-on-audio is now supported, allowing codecs that support the feature to wake the platform based on audio activity.

1.7 SMBUS

ICH4 provides an SMBus 2.0-compliant Host Controller for the CPU to initiate communications with SMBus peripherals. In addition, ICH4 is also capable of operating in a mode in which it can communicate with I2C compatible devices.

The ICH4s SMBus controller implements hardware- based PEC (Packet Error Checking). The actual PEC calculation and checking for SMBus messages with PEC enabled is performed in the hardware. The SMBus Host Controller logic can be configured to automatically append the CRC byte if configured and also performs the checking on the CRC. This relieves both the software and CPU for other tasks.

ICH4 also provides a 32-byte data buffer that greatly reduces software and CPU overhead when dealing with bus protocols involving "blocks" of data. Previously, data in a block transfer was handled byte-by-byte, needing constant polling and updating of respective status fields. This becomes a thing of the past by using the 32-byte data buffer in ICH4.

The ICH4 slave interface allows an external master to write or read to the ICH4. Write cycles can be used to communicate events or messages to other parts of the platform, and the read cycles can be used to determine the state of various status bits. In ICH4, two new status indicators were added to slave interface- the Battery Low indicator and the CPU Power Failure status.

1.8 LAN

ICH4 integrates the digital functions associated with the 82559 LAN Controller. Together with an external PHY from the Intel® 82562 Platform LAN Connect family, ICH4 provides an integrated 10BASE-T/100BASE-TX LAN solution.

The 32-bit PCI controller within the LAN function provides enhanced scatter-gather bus mastering capabilities. Two large transmit and receive FIFOs of 3 Kbyte each help prevent data under-runs and overruns. This enables the ICH4 to transmit data with minimum interframe spacing (IFS).

ICH4 LAN function can operate in either full duplex or half duplex mode. In full duplex mode ICH4 adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

ICH4 includes an interface to a serial (4-pin) EEPROM. The EEPROM provides power-on initialization for hardware and software configuration parameters. An EEPROM of 256 words is required to support the heartbeat command.

The ICH4 LAN function also provides a SMBus slave interface. The SMBus interface is used as an interface between the LAN controller and the integrated SMBus host controller. Combined with System Management function in ICH4, the LAN controller supports Basic AoL (Alert on Lan).

1.9 Other Improvements in ICH4

ICH4 includes a variety of other enhancements and new functions to improve platform performance, reduce costs, and add functionality. Examples include:

- The ICH4 has integrated a dual Hub Interface 1.0/1.5 buffer that supports a variety of MCHs.
- The ICH4 integrated IDE supports tri-state modes to enable swap bays.
- New SYS_RESET# signal. This new input signal can be connected directly to a standard front panel push-button for resetting the system. The ICH4 integrates debouncing logic so that the signal can be connected directly, saving the external logic that has been found with prior systems and allows for unambiguous reporting of reset events.
- New SLP_S4# signal. This new output signal can be used to control power to external devices that should be powered off during S4 states. This provides more flexibility in the system design.
- New THERMTRIP# signal. This new input signal is connected directly to the corresponding signal on Intel® Pentium® 4 processors. When THRMTRIP# goes active, ICH4 automatically transitions the system to low-power state where the CPU's power is shut. This saves external logic that was previously implemented on prior platforms.
- Lower core voltage. The ICH4 core runs at 1.5 V, reducing the core power required versus prior generations running at 1.8 V.